CLAIMS

1. A semiconductor structure comprising:

a semiconductor substrate;

at least one first crystalline epitaxial layer on said substrate, said first layer having a surface which is planarized; and

at least one second crystalline epitaxial layer on said at least one first layer.

2. The structure of claim 1, wherein said at least one first crystalline epitaxial layer is lattice mismatched.

3. The structure of claim 1, wherein said at least one second crystalline epitaxial layer is lattice mismatched.

4. The structure of claim 1, wherein said first and second crystalline epitaxial layers are lattice mismatched.

5. The structure of claims 2, wherein said at least one first layer comprises a composition graded relaxed epitaxial region.

6. The structure of claims 3, wherein said at least one second layer comprises a composition graded relaxed epitaxial region.

7. The structure of claims 4, wherein said first and second layers comprise composition graded relaxed epitaxial regions.

8. The structure of claim 7, wherein said at least one first layer comprises a first composition graded relaxed epitaxial region and a first uniform composition layer.

9. The structure of claim 8, wherein said at least one second layer comprises a second uniform composition layer and a second composition graded relaxed epitaxial region.

10. The structure of claim 9, wherein said first and second uniform composition layers are substantially lattice mismatched.

11. The structure of claim 9, wherein the surface of said at least one second layer comprises substantially fewer threading dislocations and dislocation pile-ups.

12. The structure of claim 9, wherein said substrate comprises silicon, and said first and second composition graded relaxed epitaxial regions and said first and second uniform composition layers comprise a Ge_xSi_{1-x} alloy.

13. The structure of claim 12, wherein the planarization occurs at a composition of approximately 50%.

14. The structure of claim 13, wherein the final Ge concentration is approximately between 70 and 100%.

15. The structure of claims 1, wherein said at least one second crystalline epitaxial layer comprises a surface which is planarized.

16. The structure of claim 15, wherein subsequent epitaxial layers are provided on said second layer, each of which comprises a surface which is planarized.

17. The structure of claim 1, wherein said first layer is planarized by chemical-mechanical polishing.

18. The structure of claim 15, wherein a first planarization occurs at approximately between 20 and 35% GeSi, and a second planarization occurs at approximately between 50 and 70% GeSi.

19. The structure of claim 12, wherein compressive strain is incorporated in said graded region to offset the tensile strain that is incorporated during thermal processing.

20. The structure of claim 1, wherein alloys of Ge_xSi_{1-x} from x=0 to about x≈35% are grown at 750°C, alloys from x=35 to about x≈75% are grown at between 650°C and 750°C, and alloys greater than 75% are grown at 550°C.

21. A semiconductor structure comprising:

a silicon substrate; and

a GeSi graded region grown on said silicon substrate, compressive strain being incorporated in said graded region to offset the tensile strain that is incorporated during thermal processing.

22. The structure of claim 21, wherein the compressive strain is incorporated by growing GeSi alloys at lower temperatures such that the alloy does not completely relax.

23. The structure of claim 21, wherein the compressive strain is incorporated by decreasing the growth temperature as Ge concentration increases in said graded region.

24. The structure of claim 21, wherein alloys of Ge_xSi_{1-x} from x=0 to about x≈35% are grown at 750°C, alloys from x=35 to about x≈75% are grown at between 650°C and 750°C, and alloys greater than 75% are grown at 550°C.

25. The structure of claim 21, wherein said graded region comprises a surface which is planarized.

26. The structure of claim 25, wherein said graded region is planarized by chemical-mechanical polishing.

27. A semiconductor structure comprising:

a semiconductor substrate;

a first layer having a graded region grown on said substrate, compressive strain being incorporated in said graded region to offset the tensile strain that is incorporated during thermal processing, said first layer having a surface which is planarized; and

a second layer provided on said first layer.

28. A method of fabricating a semiconductor structure comprising:

providing a semiconductor substrate;

providing at least one first crystalline epitaxial layer on said substrate; and

planarizing the surface of said first layer.

29. The method of claim 28 further comprising providing at least one second crystalline epitaxial layer on said first layer.

30. The method of claim 28, wherein said step of providing said first layer comprises growing a GeSi relaxed graded region on said substrate.

31. The method of claim 30 further comprising incorporating compressive strain in said grade region to offset tensile strain incorporated during thermal processing.

32. The method of claim 31, wherein said step of incorporating compressive strain comprises decreasing the growth temperature as Ge concentration increases in said graded region.

33. The method of claim 32, wherein said step of incorporating compressive strain comprises growing alloys of Ge_xSi_{1-x} from x=0 to about x≈35% at 750°C, growing alloys from x=35 to about x≈75% at between 650°C and 750°C, and growing alloys greater than 75% at 550°C.

34. The method of claim 28, wherein said step of planarizing comprises chemical-mechanical polishing.

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